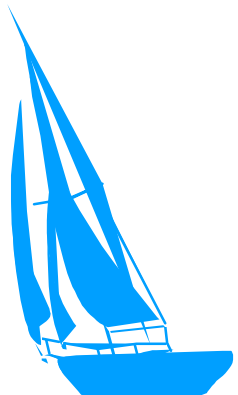




Design Automation

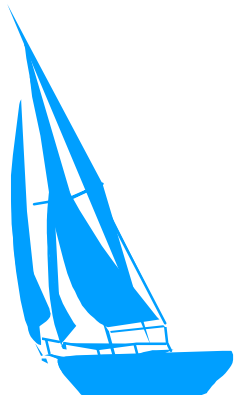
Engineering the Future





Main Areas

- ◆ Logic Simulation
- ◆ Physical Design Automation





Logic Simulation

- ◆ Levelization
- ◆ Levelized Compiled Code Simulation
- ◆ Event Driven Simulation
- ◆ Multi-Delay Simulation
- ◆ Current Research



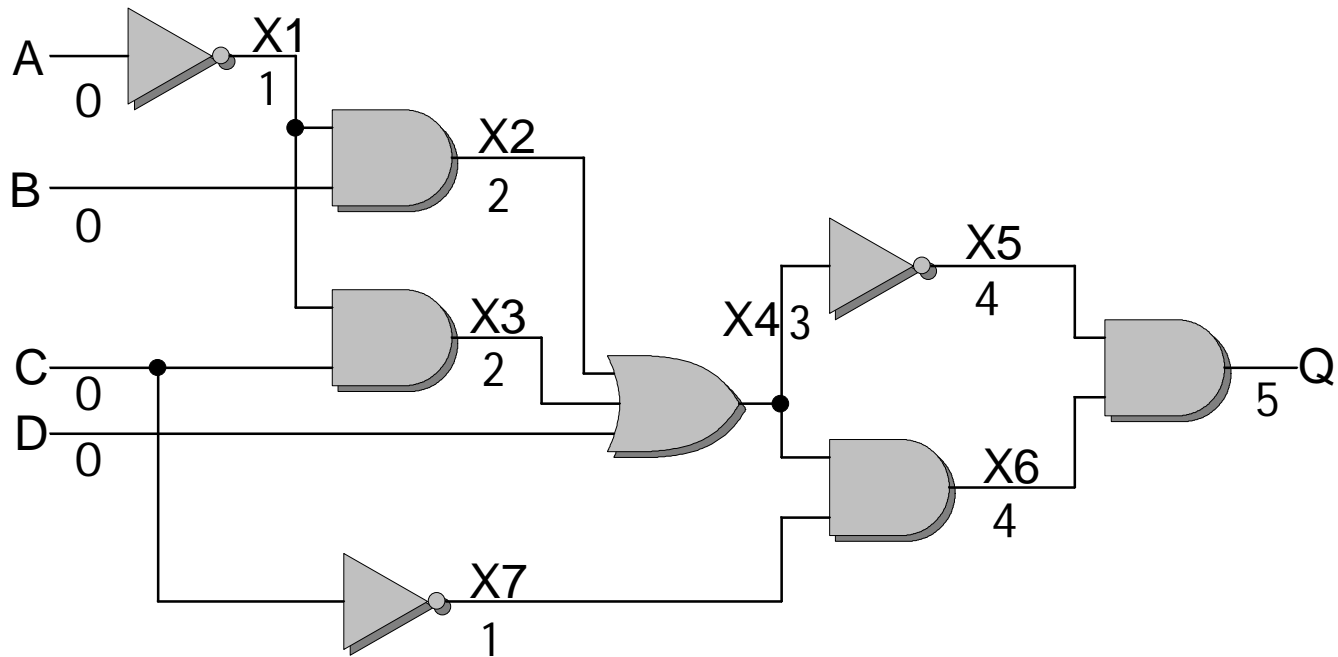


Levelization

- ◆ Assign Zero to All Primary Inputs
- ◆ If All Gate Inputs Have Level Numbers:
 - Find Maximum Level for all Gate Inputs
 - Add One to Maximum
 - Assign New Value to Gate and Its Outputs
- ◆ Special Considerations for:
 - Wired And, Wired Or connections
 - Sequential Circuits

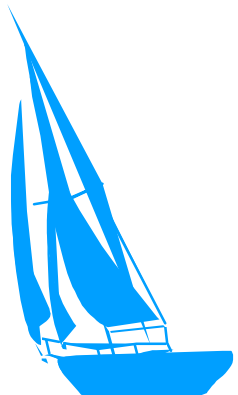
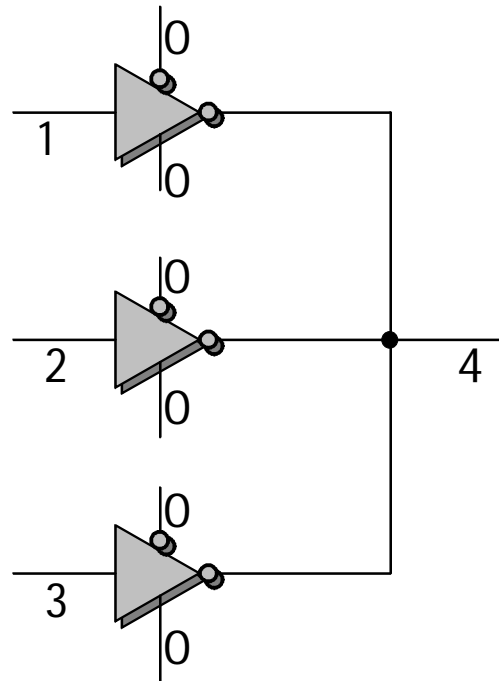


Levelization: Example

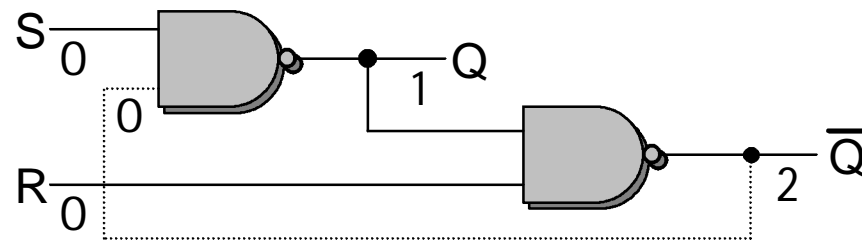
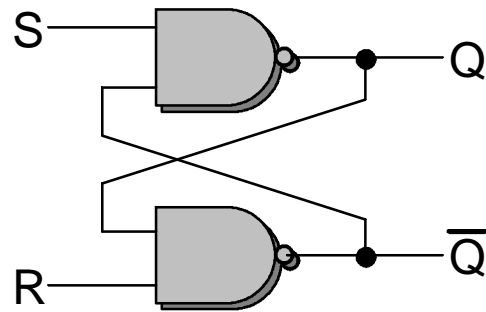




Wired-Or Connections



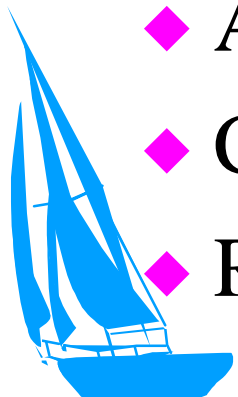
Sequential Circuits



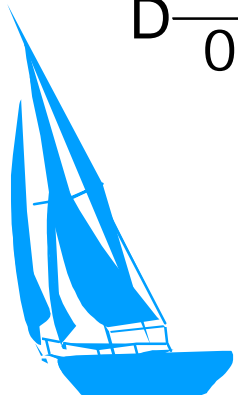
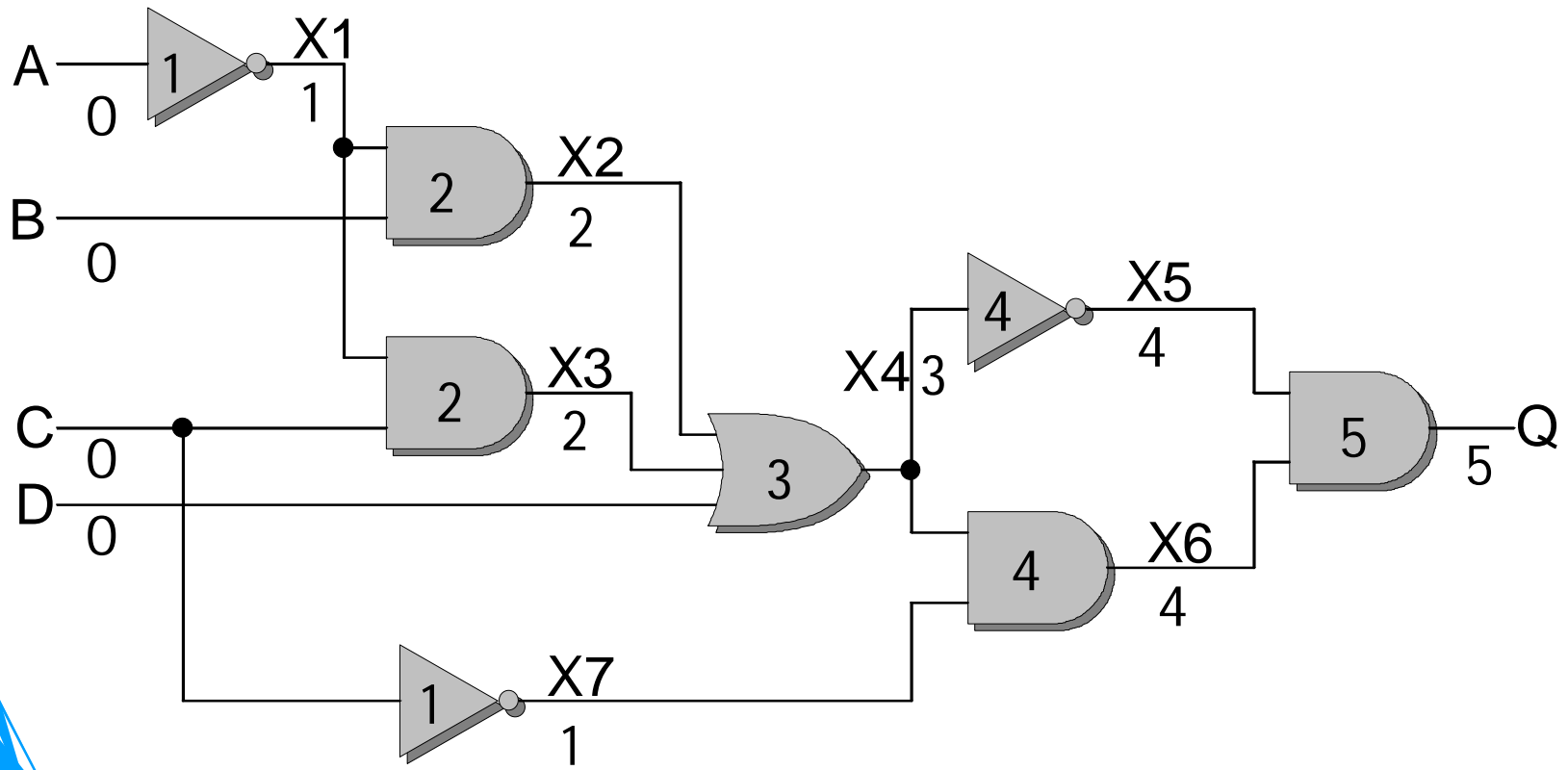


LCC Simulation

- ◆ Levelize the Circuit
- ◆ Sort Gates into Ascending Order by Level
- ◆ Generate Code for Each Gate
- ◆ Add Input/Output Routines
- ◆ Add Control Loop
- ◆ Compile Generated Code
- ◆ Run Simulator




LCC Example





LCC: Generated Code

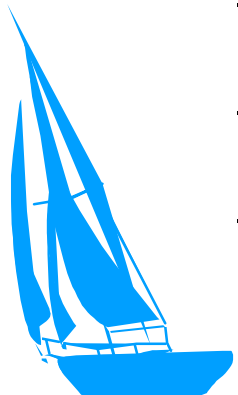
```
SimCkt()
{
    X1 = ~A;
    X7 = ~C;
    X2 = X1 & B;
    X3 = X1 & C;
    X4 = X2 | X3 | D;
    X5 = ~X4;
    X6 = X4 & X7;
    Q = X5 & X6;
}
```



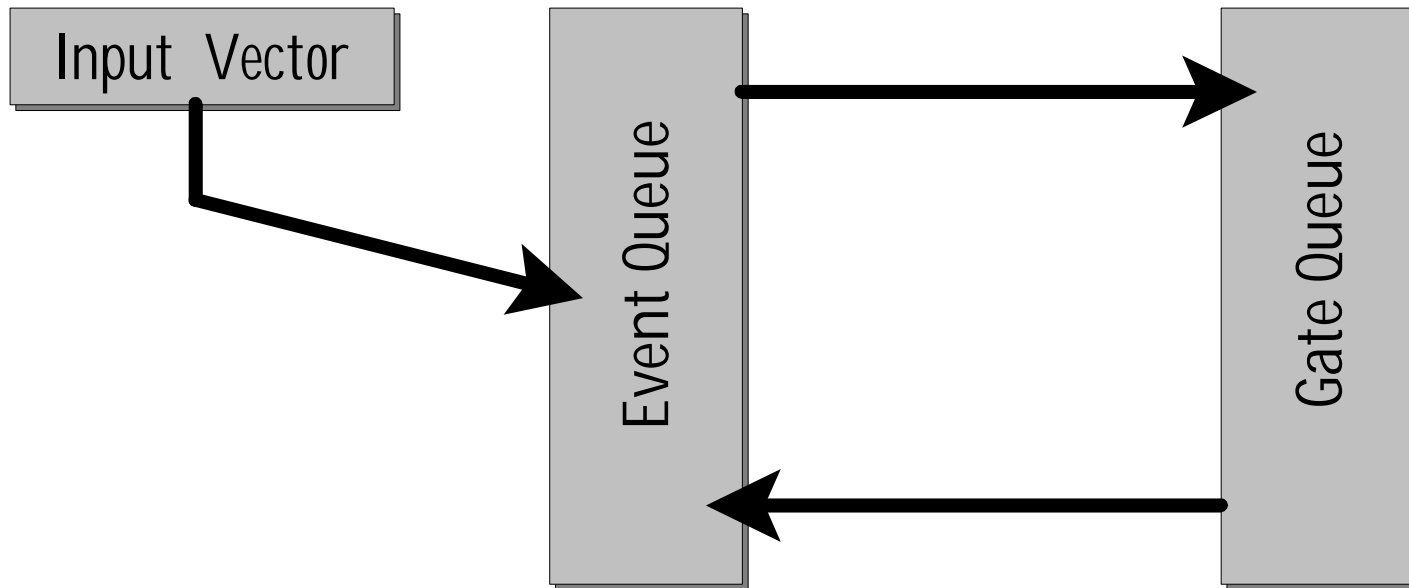


Event Driven Simulation

- ◆ Test Input Vector for Changes
- ◆ Schedule Events for Primary Inputs
- ◆ Repeat Until Finished:
 - Process Each Event, Changing Net Values
 - Schedule Gate Simulations
 - Simulate All Scheduled Gates Test Outputs
 - Schedule Events for Changed Nets



Event Driven Simulation



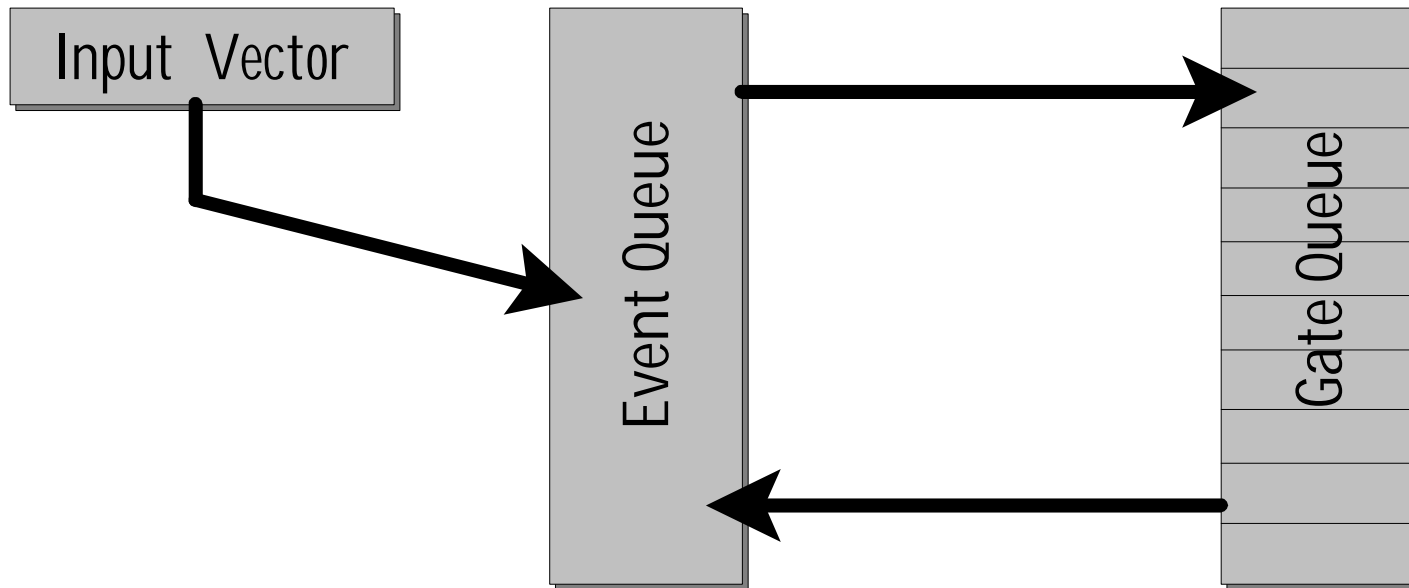


Multi-Delay Simulation

- ◆ Divide Event Queue into Time Slots
- ◆ If Max Delay is D , D slots are required
- ◆ Slots are reused for times $D+n$
- ◆ Events for time T queued in slot $T \bmod D$
- ◆ Nets Tested for Changes During Event Processing
- ◆ No Changes in Gate Processing



Multi-Delay Simulation





Recent Research

- ◆ PC-Set Method
- ◆ Parallel Technique
- ◆ Threaded Code
- ◆ The Inversion Algorithm
- ◆ BDD Techniques
- ◆ LECSIM





Physical Design Automation

- ◆ Routing

- ◆ Placement

- ◆ Partitioning



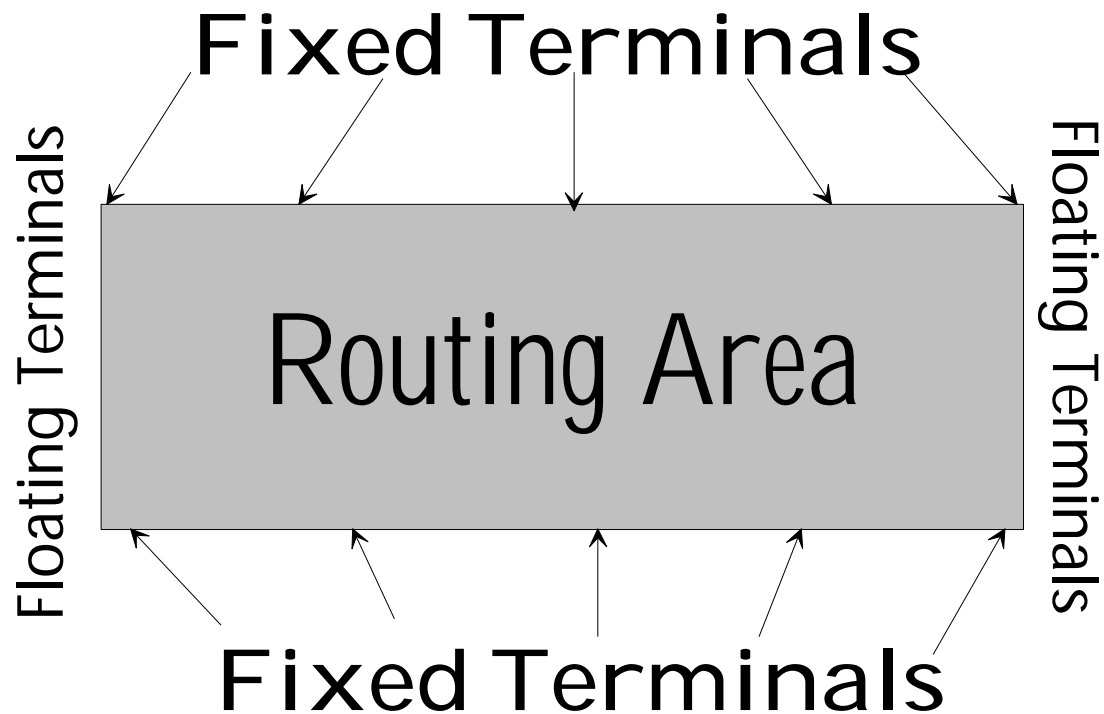


Routing

- ◆ Channel Routing
- ◆ Global Routing
- ◆ Lee Routers
- ◆ Specialized Topics

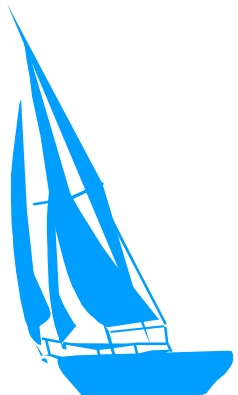
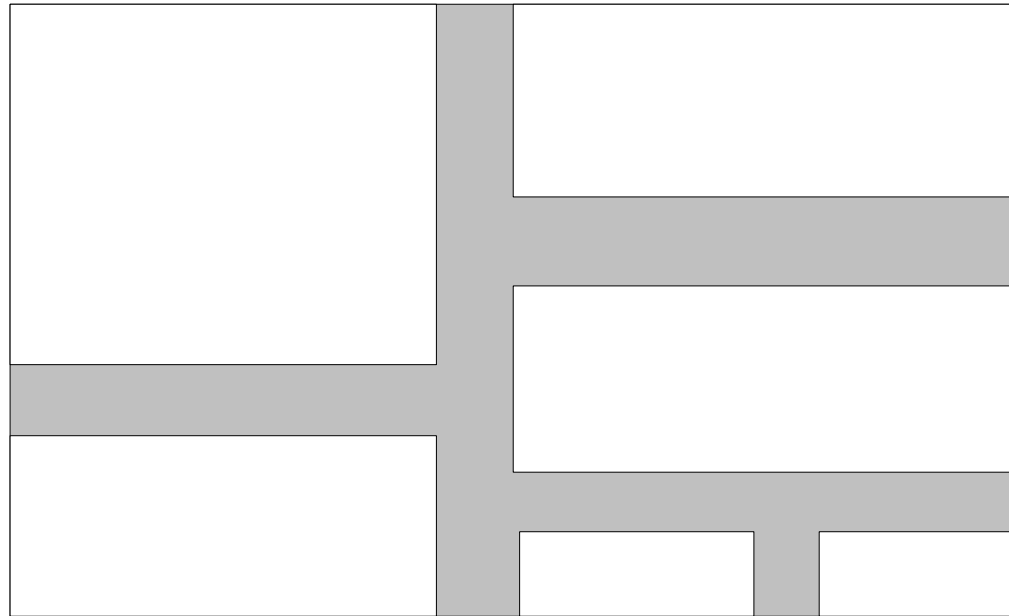


Channel Routing

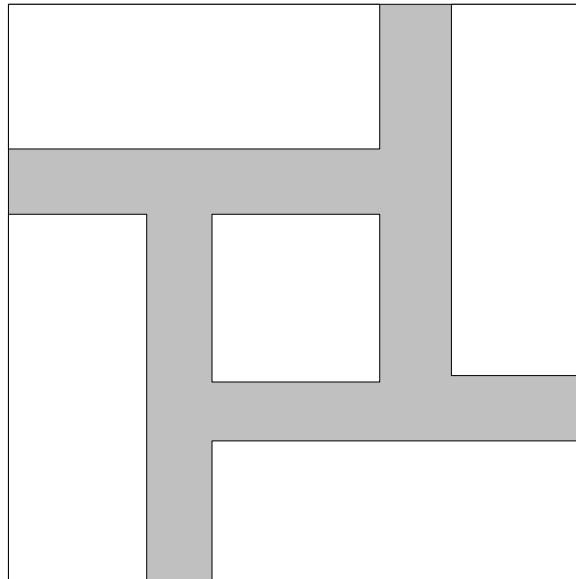




Global Routing

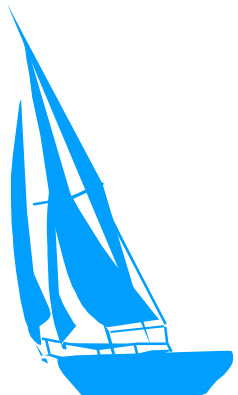
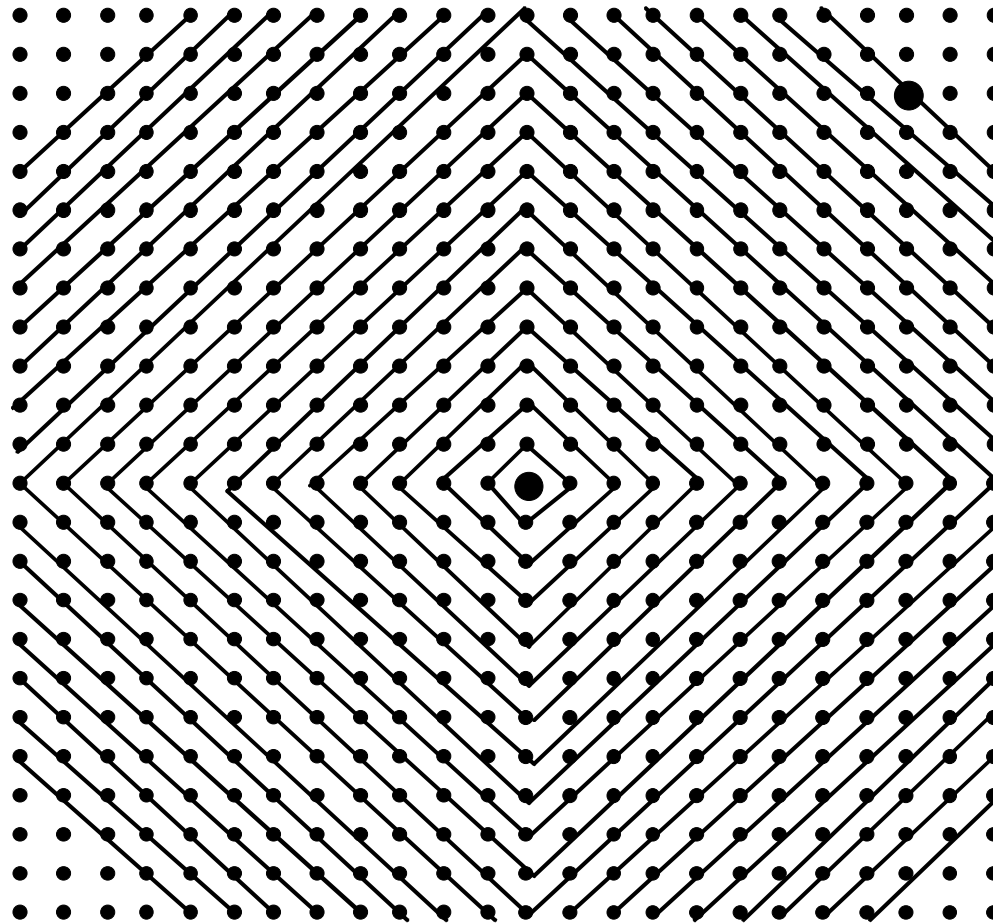


Channel Ordering





Lee Routing





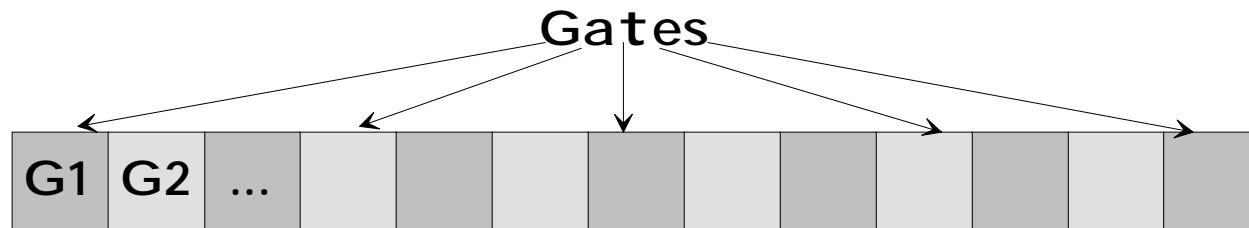
Other Routing Topics

- ◆ Switch-Box Routing
- ◆ River Routing
- ◆ Power and Ground Routing
- ◆ Clock Distribution





Placement



Routing Channel



Routing Channel



Routing Channel



Partitioning

