CIS 4930-003 **VLSI Design Automation** **Spring 97**
LIF 263 **2:00-3:15 PM MW**

Instructor: Peter M. Maurer
Office: ENB 314
Office Hours: WR 11:00-12:00 AM
Phone: 974-4758
Text: None

Examinations:
Feb 10, Mar 24, Final: Apr 25 – 3:30-5:30PM.

Topics (Not necessarily in order)	
1.Review of Logic Design	14. The convergence algorithm
2.Logic models, and gate-level simulation	15. The sync and async parallel techniques
3.Levelization, and LCC simulation.	16. The gateway algorithm
4.C programming principles	17. The shadow algorithm
5.Windows Programming and DLLs	18. Multi-Delay Compiled Simulation
6.VB Programming	19. The multi-delay parallel technique
7.VBX Programming	20. The Inversion Algorithm
8.Unit-Delay Simulation	21. Three-valued Inversion Algorithm
9.Multi-Delay Simulation	22. Unit-Delay Inversion Algorithm
10.Compiled Event-Driven Simulation	23. Parallel Simulation
11.The PC-Set Method of UD Sim	24. Partitioning
12.The parallel technique of UD Sim	25. Fault Simulation
13.LECSIM compiled levelized simulation	26. Backsim

There will be three equally weighted exams, given on the dates indicated. These three exams will constitute 85% of your final grade. In addition, there will be homework exercises, which will constitute 15% of your grade. I have an open-door policy with respect to office hours. You may come to my office at any time. I habitually keep my office door closed and locked. Don't be afraid to knock.

If I were alive today, I'd definitely be taking Dr. Maurer's Design Automation Course!