This is a list of files and the titles of the TRs they contain
The code preceding each file name is the technical report number,
and the number following is the year of publication.
The proper reference for the tech report "The Florida Hardware Design
Language" would be "University of South Florida, Department of Computer
Science and Engineering, Technical Report Number DA-3, 1989."

SE-1 DGL.Impl 1991
THE DESIGN AND IMPLEMENTATION OF A
GRAMMAR-BASED DATA GENERATOR

DA-1 Doorways 1991
GATEWAYS: A TECHNIQUE FOR ADDING
EVENT-DRIVEN BEHAVIOR TO COMPILED
UNIT-DELAY SIMULATIONS

DA-2 Dyn.Tstg 1990
DYNAMIC FUNCTIONAL TESTING FOR VLSI
CIRCUITS

DA-3 FHDL 1989
THE FLORIDA HARDWARE DESIGN
LANGUAGE

SE-2 Gen.Tst.Data 1990
Generating Test Data with Enhanced Context Free Grammars

DA-4 LevGate 1991
USING GATEWAYS WITH LEVELIZED
COMPILED SIMULATION

DA-5 HDL.driv.layout 1989
HDL DRIVEN CHIP LAYOUT WITHIN THE
FHDL DESIGN FRAMEWORK

DA-6 MD.Sim 1990
MDCSIM: A COMPILED EVENT-DRIVEN
MULTI-DELAY SIMULATOR

DA-7 MD.comp 1991
TWO NEW TECHNIQUES FOR COMPILED
MULTI-DELAY SIMULATION

DA-8 Multi-Lev.Sim 1989
TECHNIQUES FOR MULTI-LEVEL COMPILED
SIMULATION

DA-9 Opt.Par 1990
OPTIMIZATION OF THE PARALLEL
TECHNIQUE FOR COMPILED UNIT-DELAY
SIMULATION

DA-10 Route.Tut 1990
AUTOMATIC ROUTING OF INTEGRATED
CIRCUIT CONNECTIONS: A TUTORIAL

DA-11 Shadow 1991
THE SHADOW ALGORITHM: A SCHEDULING
TECHNIQUE FOR BOTH COMPILED AND
INTERPRETED SIMULATION

DA-12 Sked.HL.Blk 1988
SCHEDULING HIGH-LEVEL BLOCKS FOR FUNCTIONAL SIMULATION*

DA-13 Symm.Func 1988
THE COMPLEXITY OF DETECTING
SYMMETRIC FUNCTIONS

DA-14 UD.Comp.Cyc 1991
COMPILED UNIT-DELAY SIMULATION FOR
CYCLIC CIRCUITS

DA-15 UD.Comp.Sim 1989
TECHNIQUES FOR UNIT-DELAY COMPILED
SIMULATION

DA-16 UD.Comp2 1991
TWO NEW TECHNIQUES FOR UNIT-DELAY
COMPILED SIMULATION

DA-17 UD.Sim.Cyc 1990
COMPILED UNIT-DELAY SIMULATION FOR
CYCLIC CIRCUITS

DA-18 alogic 1989
THE FHDL MACRO PROCESSOR

DA-19 cosim 1988
COSIM: AN EXPERIMENTAL CONCURRENT FAULT
SIMULATOR

DA-20 lecsim 1989
LECSIM: A LEVELIZED EVENT DRIVEN
COMPILED LOGIC SIMULATOR

DA-21 plasm 1989
THE FHDL PLA TOOLS

DA-22 romasm 1989
THE FHDL ROM TOOLS

DA-23 skedcomp 1991
SCHEDULING BLOCKS FOR
HIERARCHICAL COMPILED SIMULATION