COSIM: An Experimental Concurrent Fault Simulator

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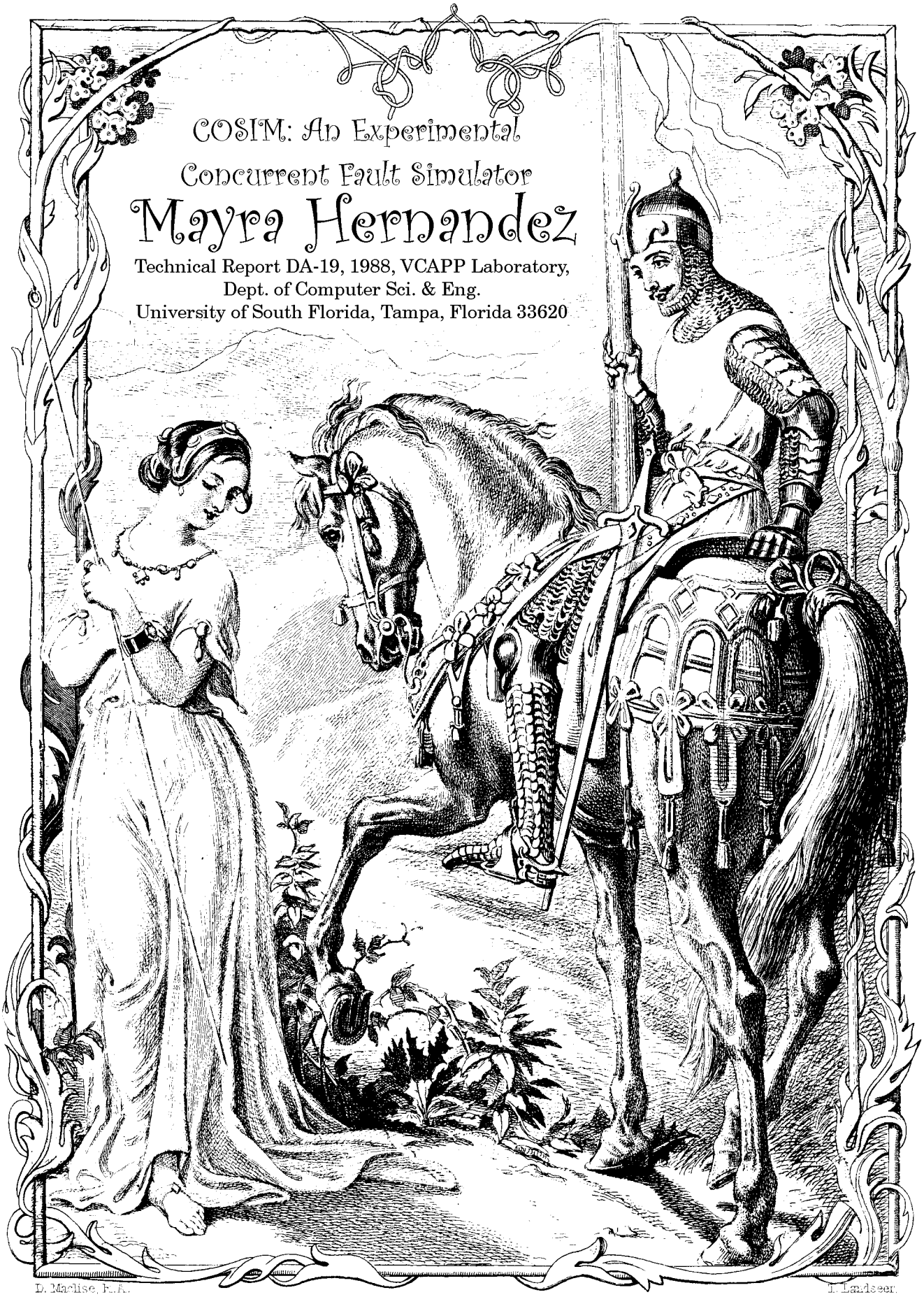

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EXTENDED ABSTRACT

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1. INTRODUCTION

Simulation is a process through which it is possible to study how different parts of a system interact without actually implementing a system or even a prototype.It is important because building and testing a prototype is time consuming and expensive. If the prototype does not comply with the requirements of a project, making changes to it or rebuilding it can use a great deal of valuable time whereas a simulator can be changed easily and quickly.

A fault simulator can help designers improve the quality and testability of circuits by helping to construct input vectors that will be used to test the final product. Concurrent fault simulation [Ulr 69] [Ulr 73] [Ulr 74] [Ulr 80] is the most efficient of the known methods for fault simulation. It was chosen for implementing the experimental fault simulator: *cosim*. *Cosim* is one of a series of CAD tools currently under development at the Department of Computer Science and Engineering of the University of South Florida.

2. COSIM

The *cosim* experimental fault simulator simulates faults in networks at the logic level. Seven types of gates can be analyzed: AND, OR, NOT, NAND, NOR, XOR, and XNOR. All of these functions are implemented using three-valued logic using the values 1, 0, and "don't know". The input files for *cosim* are designed following the syntax specifications of Maurer [Mau 88], which allows gates and nets to be declared, and allows faults to be attached to the inputs and outputs of a gate. Gates for which faults have been specified are called *fault origins*.

Cosim applies each test vector to the inputs of the gate network. The inputs of each fault-free gate are analyzed according to the gate type and an output is evaluated, and faults are (possibly) propagated to other gates using a mechanism called the *fault effect*. When a fault is propagated to a primary output, the fault has been detected.

Cosim uses the zero delay model to simulate circuits, which implies that all simulated gates take the same amount of time to produce their outputs, and that these outputs are produced in zero time. If any signals have the unknown value after the first pass, additional passes are performed to stablize these signals. Subsequent passes simulate only those gates required to stablize the unknown signals. Multiple passes are used to simulate circuits with feedback loops such as RS flip-flops.

After all of the input vectors have been exhausted, a report of all detected and undetected faults is generated.

There are several potential enhancements that could be made to *cosim*. Among these are the use of a unit delay or a variable-delay model instead of the zero-delay model, inclusion of other types of faults in addition to the classical stuck-at-one/stuck-at-zero faults, and performance enhancements such as removing detected faults for all vectors following the one that detects the fault. The logic model could be enhanced to include the high-impedence state.

3. CONCLUSION

Cosim is a logic simulator that can be used to verify logic models of circuits and to obtain fault-coverage information for physical test vectors. The *cosim* concurrent fault simulator is a useful design tool that is proving to be valuable addition to the collection of CAD tools available at the University of South Florida. In addition it will serve as a basis for further research in logic and fault simulation.

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